Design and Implementation of an Improved Controller for Parallel-Connected 400 Hz Frequency Converters

B. Tamyurek
Department of Electrical Engineering
Eskisehir Osmangazi University
Eskisehir, 26480 Turkey
btamyurek@ogu.edu.tr

E. Birdane, A. Ceyhan
Kaynak Electronic Machine Industry and Trade Co. Ltd.
Eskisehir, Turkey
{birdane, aceyhan}@kemsan.com.tr

***Abstract*—This paper presents the design and implementation of parallel connected 400 Hz frequency converters that supply power to military equipment. Achieving tight steady-state and transient voltage regulations and high efficiency in inverters with high fundamental frequency presents great challenge both on the control system design and the power stage design. This study develops and implements a controller with paralleling functions that achieves the stringent power quality requirements. It also includes developing the circuit models of the controller and the converter stage, and finding the optimum design based on the simulation results. Then, experimental work is performed on the converters built at the rated power to validate the design. Finally, the test results demonstrate that the developed control system and the converter design achieve the desired specifications demanded by the military applications.**

I. INTRODUCTION

Some equipment used in aircrafts and naval ships need frequency converters to interface to the ground electric power system which is either fed from 50/60 Hz utility mains or from a variable frequency diesel generator. These converters are installed to provide an output voltage of $115\,\mathrm{V}$ or $440\,\mathrm{V}$ at a constant frequency of 400 Hz. The type of power defined in the interface standard for ship board systems is classified into three types, based on the frequency of the output voltage: type I is 60 Hz power and type II and III are 400 Hz power [1]. According to the standard, the difference between type II and type III power is that type III has more stringent steady-state and transient voltage regulation requirements than the other. Achieving tight regulations and high efficiency in inverters with high fundamental frequency presents great challenge both on the control system design and the power stage design of the converter. However, the objective of this study is to realize such a system and produce a product that supplies high quality AC power to the military loads. Moreover, direct paralleling of converters is desired in most applications. So, this study also includes developing and implementing an effective and reliable paralleling strategy.

The single line diagram of a typical parallel connected type III frequency converter system, which is also the system to be implemented in this work, is shown in Fig. 1. The major difficulty in the design of existing 400 Hz frequency converters is to achieve a low total harmonic distortion (THD) while maintaining a tightly regulated sinusoidal output voltage [3]. Also, a good waveform quality with perfect synchronism is important if direct paralleling of converters in voltage mode is desired.

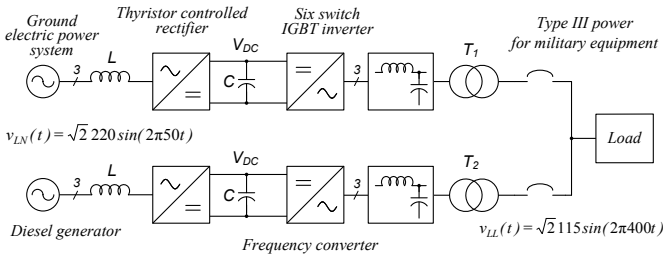
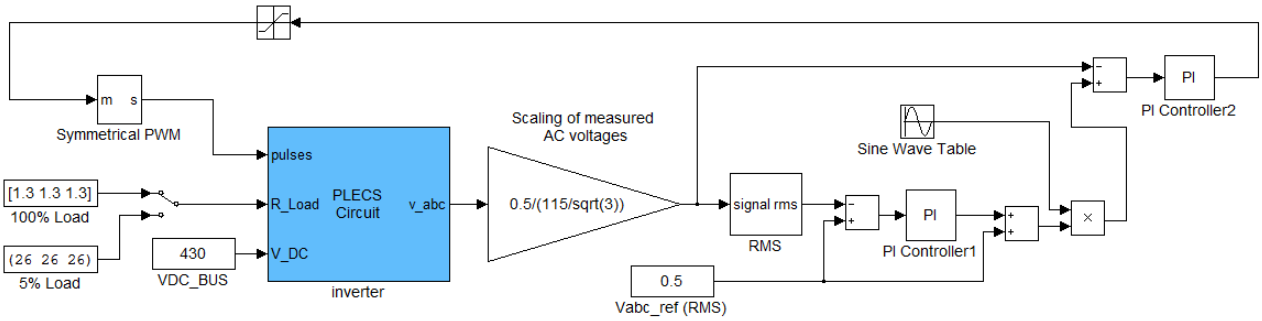
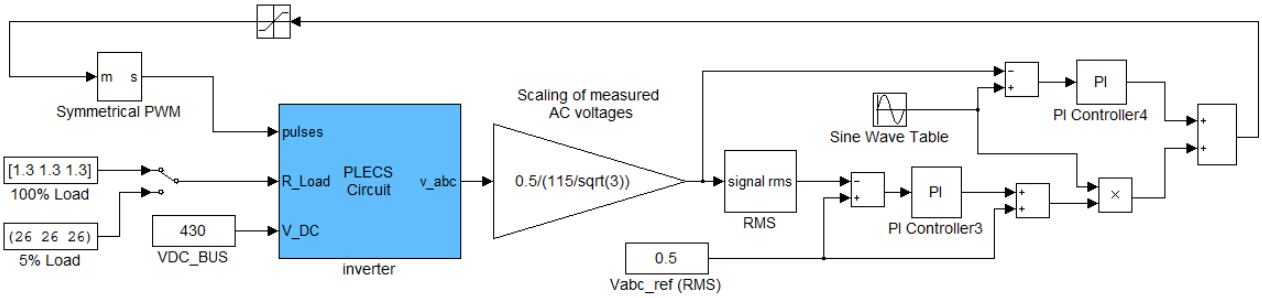


Fig. 1. The single line diagram of a ground electric power interface system including two parallel connected 400 Hz frequency converters.



(a)



(b)

Fig. 2. The Simulink model of the control system: (a) the classical SPWM method and (b) the improved SPWM controller.

Research so far has shown that some improvements must be made on the classical control techniques, such as the sinusoidal PWM (SPWM) and the space vector PWM (SVPWM) to meet the regulation requirements of the mid frequency converters [3]-[11]. The frequency modulation ratio m_f is typically less than 25 for frequency converters. The excess switching losses in IGBTs put an upper limit to the maximum switching frequency [2]. So, the design of a controller with low m_f results in a lower controller bandwidth which causes steady state error in the output voltage and a slower dynamic response. Some research has effectively increased the switching frequency by using full-bridge topology for each phase leg [3]-[4]. Unipolar voltage PWM switching of the bridges doubles the switching frequency in the inverter legs. The drawback of this technique is the usage of more semiconductor devices [5]-[6]. We propose an improved controller, which is shown in Fig. 2, to increase the bandwidth without increasing the switching frequency and changing the topology. Additionally, the proposed controller strategy is more convenient for digital implementation made with fixed point DSPs than the classical method. The next section discusses the control system and its advantages.

II. CONTROL SYSTEM

Specifications require that the converter should be operable both as a three-phase and also as a single-phase power source. For this reason the sinusoidal PWM method is used for the control system, since it allows independent control of each phase. Fig. 2 shows the Simulink models of the classical SPWM and the proposed improved SPWM methods. The problem with the low bandwidth at 400 Hz designs can be improved by modifying the inner AC voltage loop of the classical system. The following sections will describe each method.

A. Description of Classical SPWM Control System

As shown in Fig. 2(a), in the classical two loop control method, the output of the outer voltage loop, which are the compensated RMS voltage errors for each phase, is multiplied by the reference sine wave tables, and reference AC signals are generated. Then, these signals are compared to the measured AC voltages and errors are detected. Finally, the detected errors are fed into PI regulators which produce the modulating control signals for each phase. The modulating signals are the inputs to the symmetrical PWM block as shown in Fig. 2(a), where they are compared to the triangular waves for PWM generation.

B. *Description of Improved SPWM Control System*

In the proposed improved control system, as shown in Fig. 2(b), the measured AC voltages are directly compared to the reference sine waves and the detected errors are fed into PI regulators, which generate the control signals that are responsible for the waveform correction of the output voltages. In other words, these signals independently affect and control the THD of the output voltages and correct the phase difference in the waveform. The RMS magnitude correction comes from the outer voltage loop. Finally, the two control signals are added together to generate the main modulating control signals for the PWM generation.

The bandwidth improvement in this control system is obtained by separately controlling the RMS magnitude of the output voltages using the outer DC feedback loop and separately controlling the THD using the inner AC feedback loop with the help of the reference sine wave tables. The only criterion is that under the nominal steady-state operating conditions, the magnitude of the sine waves in the table must be equal to the scaled magnitude of the desired output voltages. For example, the magnitude of the measured AC voltages in the simulation as shown in the Simulink model of Fig. 2 is 0.7071 after the scaling block when the actual voltage is 115 V_{LL} (RMS), and so the magnitudes of the sine waves in the table must be equal to this value.

Separating the control loops also provides a great deal flexibility and simplification during the digital implementation of the control system with fixed point DSPs. When the waveforms in Figs. 3 and 4 are compared, it is explained how the digital implementation benefits from the improved control structure. Fig. 3 shows the simulated waveforms of the classical control, where (a) are the signals coming into the PI controller2 and (b) are the signals generated. The signals in (b), which indicate a voltage modulation ratio (m_a) of 0.8, are compared to triangular waves to generate PWM pulses. The magnitude of the ripple in (a) is multiplied by the gain of the PI controller, and any attempt to modify the ripple affects the steady-state behavior and the dynamic response of the system. An attempt to reduce the ripple at the output voltage results in slower dynamic response and poor voltage transient regulation. However, we are able to eliminate this problem using the proposed control system.

Fig. 4 shows the simulated waveforms of the proposed controller, where (a) shows the signals coming into the PI controller4 (see Fig. 2(b)), which are mainly the ripple part of the measured AC voltages, but also include information about the phase difference, (b) shows the signals generated by the PI controller4, (c) is the output of the outer voltage loop indicating an m_a of 0.8, and finally (d) shows the modulating control signals. Since the modulating control signal is the addition of compensated AC error (ripple) and the compensated RMS voltage error in the improved method, the independent control of ripple without sacrificing the system dynamic response is possible. First, the steady-state error and the transient voltage regulation are optimized by adjusting the parameters of the PI controller3, which compensates the RMS voltage error. Then, parameters of PI controller4 are adjusted to obtain the best ripple and waveform quality without affecting the dynamic response significantly.

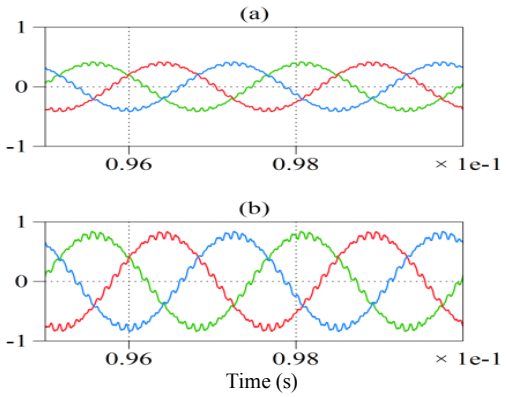


Fig. 3. The simulated waveforms of classical control system: (a) the signals coming into and (b) the signals generated the PI controller2.

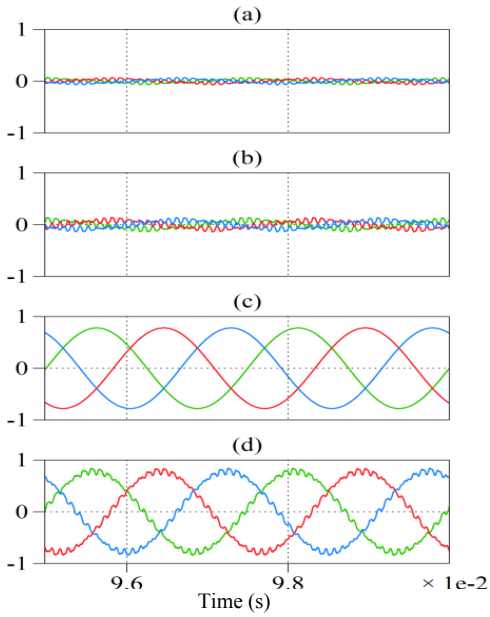


Fig. 4. The simulated waveforms of proposed control system: (a) the signals coming into and (b) the signals generated by the PI controller4; (c) output of the outer voltage loop and (d) the modulating control signals for each phase.

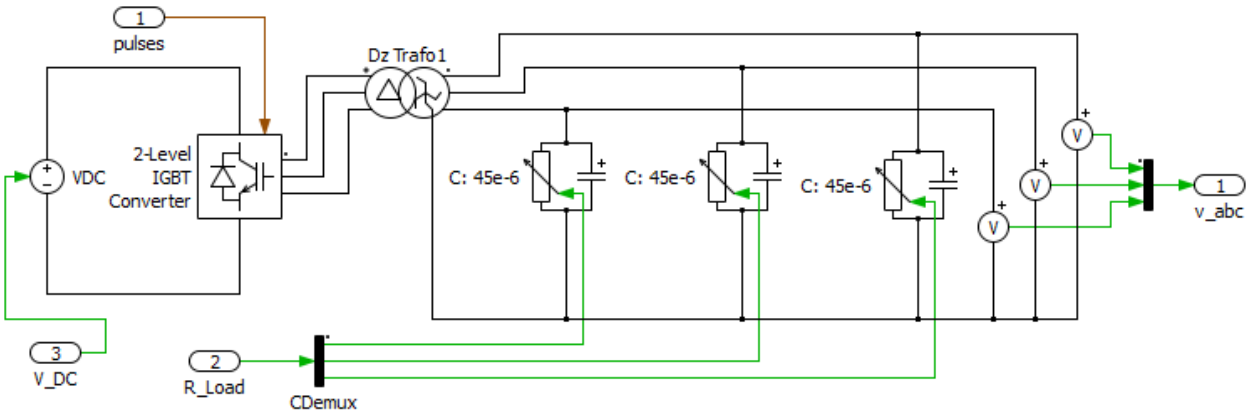


Fig. 5. The PLECS circuit model of the inverter, the transformer, and the output LC filter used in the simulations.

C. *Paralleling Strategy*

There are various methods available to use for direct paralleling of converters. However, we prefer the master-slave approach because it is easier to implement and provides very good load sharing. In this approach, both units behave like two voltage sources. The drawback of this approach is that there has to be a communication link between the paralleled units. One more problem, as also reported in the literature, is the requirement for the continuous supply of load in case of an error, such as failing of the master unit and/or broken communication link. Nevertheless, the needed precautions are implemented within our proposed control system. When the control system detects a fault in the master unit, the slave unit quickly becomes master and keeps supplying power to the load. Also the main controller always checks for the quality of the data transfer across the communication link. When a broken communication link is detected, the main controller maintains the system to operate independently as unparalleled units. In other words, the converters are not shut down, but they work as two master units. In this case, appropriate switching elements installed externally will physically isolate the output power of the units from each other. The following paragraphs describe the communication and paralleling strategy in detail.

The cable placed on the top of the converters as shown in Fig. 6 is a RS485 interface. The length of this cable is 50 meters. On this interface, we transmit the following signals:

The modulating control signals for each phase, which are the signals compared to the triangular waves for PWM generation. The data are transferred at every $100\,\mu s$ and with a 1.5Mbps transfer rate. In this paralleling strategy, both units work as voltage sources and the outputs of the converters are directly connected. For this reason generating sinusoidal voltages with perfect synchronism is important to achieve good power and current sharing. This is only obtained when the triangular waveforms on both units are synchronized. At the end of the every data transfer, when the last data bit has arrived, the controller of the slave unit synchronizes its triangular waveforms with the master.

Besides synchronization of triangular waveforms, the magnitudes of the output voltages must be the same to provide equal power sharing. The output voltages will not be equal when the DC bus voltages are not the same. Therefore, the next data that must be transmitted is the DC bus voltage information. The correct voltage modulation ratio for the slave unit is calculated using the DC bus voltage of the master unit. The modulation ratio of the slave unit is divided by the ratio of the DC bus voltages for the equalization of output voltages.

Finally, the last data is the unit's fault information. When any one of the units receives such information, that unit automatically becomes a master and continues to operate as long as the supplied load is within the rated limits of the converter. Moreover, when the faulted unit is reenergized or the error is cleared, the unit first monitors the communication port to see the existence of any master unit by checking the data on the bus. If the presence of a master unit has been detected through the received data, the unit will start as slave; otherwise it will start as master.

III. Design of The Converter

A. *Converter Design Specifications*

This project requires two 10 kVA converters operating in parallel mode. The converters will be installed on a warship, and the distance between the

units will be 50 m. Each unit requires an isolation transformer at the output. The voltage at the load side is 115 V line-to-line. The type III power specifies the worst case voltage tolerance as ±5% around the nominal voltage if the event duration is less than 250 ms and specifies the user voltage tolerance as ±1% with no limitation on time. Moreover, the frequency tolerance of the output voltages should be ±0.2% and the THD should be less than 3% [1].

B. Description of Converter Power Stage

As shown in Fig. 1, the front end of the converter is a three-phase thyristor controlled rectifier which regulates a constant voltage at 430 V. This voltage yields an m_f around 0.756 to regulate 115 V_{LL} at the output and it is the optimum to get a good transient response. The converter uses a 2-level three-phase IGBT inverter for frequency conversion. The modulated DC bus voltages are applied to the primary side of the isolation transformer as shown in Fig. 5. The transformer is a delta/zig-zag connected three-phase custom wound transformer. The transformers are wound in such a way that the internal leakage inductance becomes equal to the desired output filter inductance of 150 μH. The filter capacitance value is 45 μF per phase. These values provide a corner frequency of 1937 kHz for the output LC filter. Finally, the switching frequency of the PWM operation is selected as 10 kHz to meet the efficiency expectations. The control system was implemented with a Texas Instruments fixed point DSP, which is TMS320F2808.

IV. EXPERIMENTAL RESULTS

The two 10 kVA converters as shown in Fig. 6 have been specifically built and tested to investigate the performance of the proposed control system and the paralleling method. A HIOKI 3196 power quality (PQ) meter has been used to monitor and evaluate the system. Fig. 7 shows the transient response of the converter to various sag and swell events recorded by the PQ meter when a 8 kW resistive load has switched in and out during dynamic response tests. Notice that almost all the events fall within the limits of the type III power. However, there are 2 events violating but very close to the limits. Fig. 8 shows the three-phase voltages and currents, (a) when the load is applied, and (b) when the load is removed.

Fig. 9 shows the profile of the RMS voltage (a), the THD of the voltage (b), and the RMS current (c) as measured by the PQ meter for one phase of the converter during the dynamic response test. As shown in Fig. 9(a), the RMS voltage stays within the steady-state limits during sudden load changes, which is ±1% of 66.4 V. Similarly, in Fig. 9(b), the THD of the voltage is always below 2.4% when the converter is unloaded, and it is even better when under load. These values are lower than 3% specification.

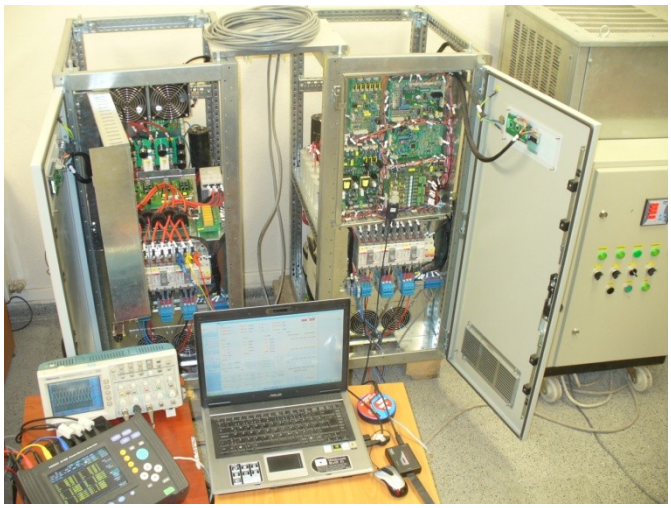


Fig. 6. The experimental step up for two 10 kVA parallel connected frequency converters.

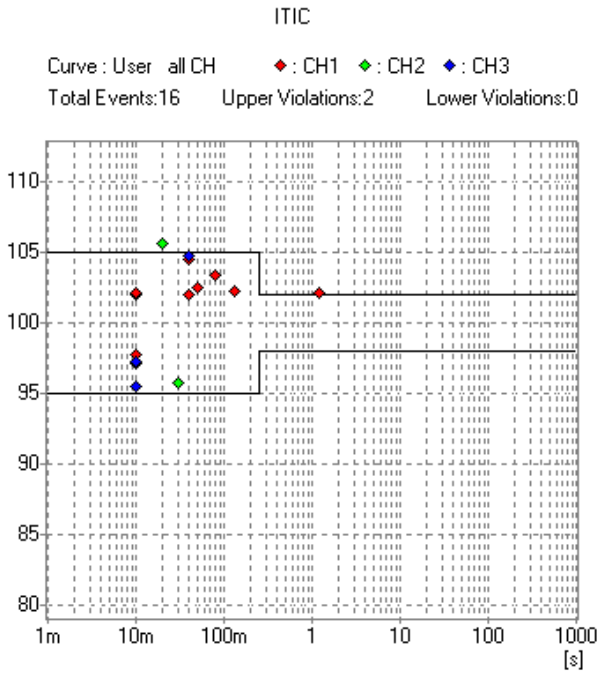
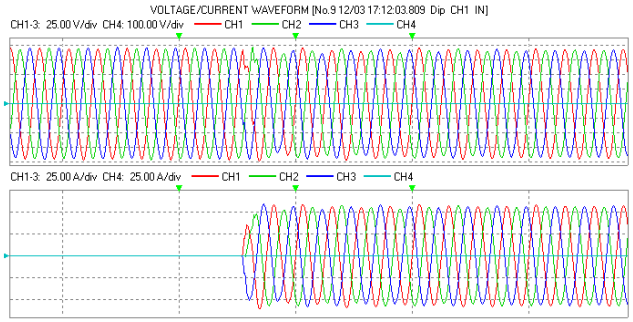
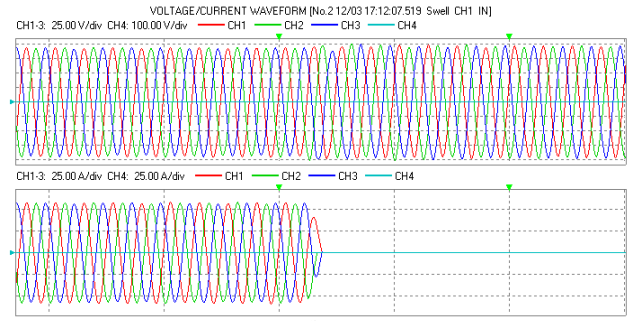


Fig. 7. The records of events occurred during dynamic response tests.

Figs. 10 and 11 show the output voltages and the currents for the same phase of the converters during the parallel operation functionality tests. Fig. 10 shows the waveforms while the master unit supplies the full load power, the slave unit is energized and shares the load current. As shown in Fig. 10, a perfect load sharing is achieved. Fig. 11 shows the waveforms during the fault tests; in (a) a fault occurs in the slave unit and it shuts off, and in (b) a fault occurs in the master unit and it shuts off. The results confirm that the load is always supplied when one of the units fails or shuts down for any reason. However, there is an unavoidable delay in the control when the master unit is shutting off as shown in Fig. 11(b). Nevertheless, this delay only lasts for one cycle, which is 2.5 ms. Note that the small currents drawn by the units after they shut off are due to the filter capacitors at the output.

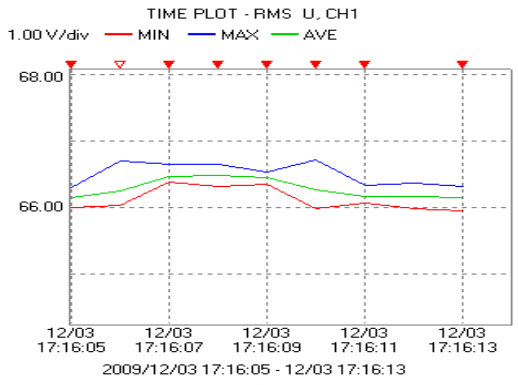


(a)

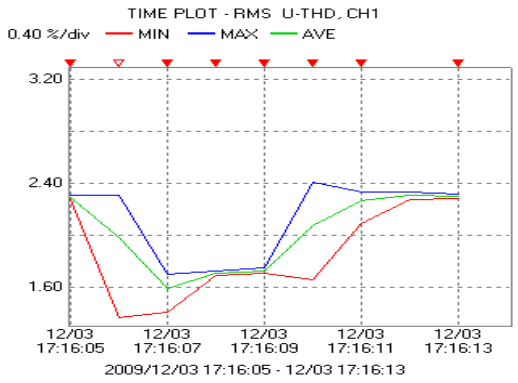


(b)

Fig. 8. The three-phase voltages and currents: (a) when the load is applied, (b) when the load is removed.



(a)



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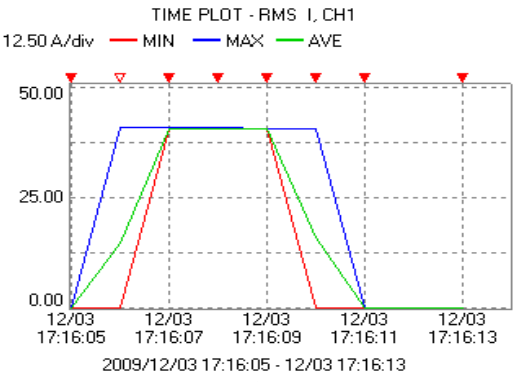


(c)

Fig. 9. The PQ meter recordings during a dynamic response test: (a) the profile of the RMS output voltage for one phase, (b) THD of the voltage for the same phase, and (c) the RMS current.

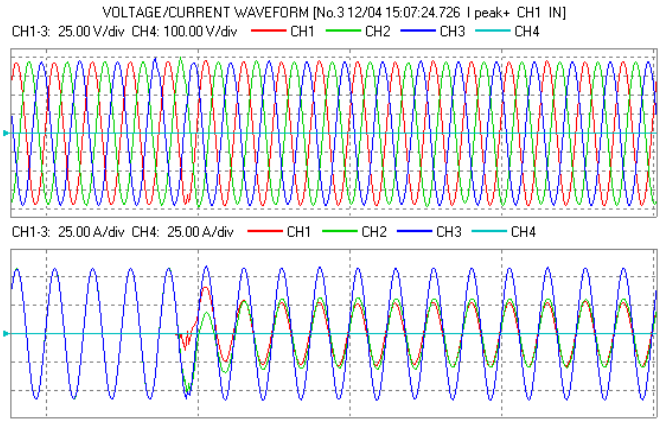
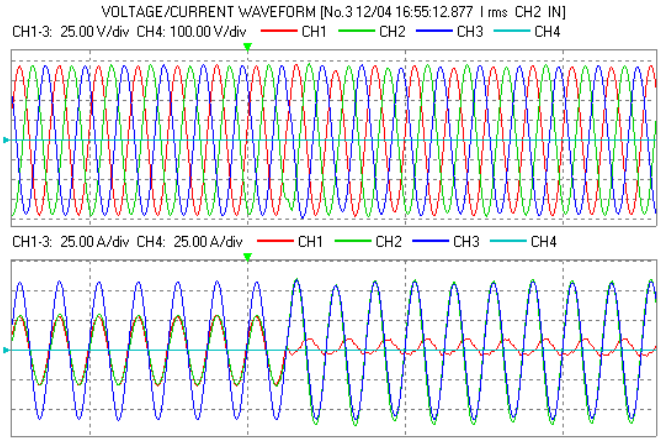
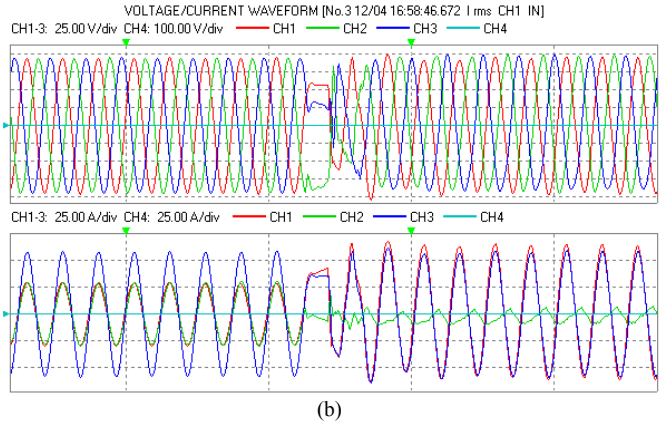


Fig. 10. The voltages (upper trace) and the currents (lower trace) when slave unit is energized while the master is supplying the full load. The CH1 is the slave current, CH2 is the master current, and CH3 is the total load current.



(a)



(b)

Fig. 11. Parallel mode failure tests: (a) The fault in the slave unit and (b) the fault in the master unit.

V. CONCLUSIONS

The objective of this study is to design digitally controlled parallel connected 400 Hz frequency converters for the military applications that need type III power. The converters provide an interface between the military equipment and either the ground electric power system or a diesel generator. The high fundamental frequency of the output makes the converter and the controller design a challenging job. So, the study includes developing a control system and finding an optimum power circuit design that achieves the stringent requirements of type III power. Controller design is done by MATLAB software, using the developed Simulink model of the control system and the PLECs model of the inverter. Then, a master-slave paralleling strategy is implemented and tested for optimum power sharing and maximum reliability. It is important to operate parallel connected systems in such a way that the power supplied to the load is not interrupted when paralleling functionality has been broken. Finally, the design is verified experimentally on two parallel connected 10 kVA converters. The results demonstrate that proposed control system, the converter design, and the paralleling strategy achieve the desired specifications and that the converters can serve the need for the intended application.

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